INVALIDATION OF INSTRUCTION CACHE LINE DURING RESET HANDLING

Abstract of the Disclosure

Methods and apparatus are provided for handling events such as faults and resets. Specialized circuitry or hardware is provided within a processor to invalidate the cache line associated with the processor cache reset address. Based on the invalided state of the cache reset address line, the processor obtains new instructions from data memory. The new instructions can be configured to invalidate the remaining cache lines using software mechanisms.